Power Adaptive Computing System Design in Energy Harvesting Environment

Qiang Liu[1], Jun Wen Luo[2], Terrence Mak[2], Wayne Luk[1], Alex Yakovlev[2]

[1]Department of Computing, Imperial College London, UK

[2]School of Electrical, Electronic and Computer Engineering, Newcastle University, UK

1. Introduction and Motivation

Traditional energy storage system has the drawback that can not working in long time due to the limitation of battery or ultra capacitors. With advances in energy harvesting system, it is possible to implement a self – powered system that harvests ambient energy from environment such as solar, vibration and wind. Such energy harvesting system provides a promising alternative to battery powered system and creates an opportunity for architecture and design method innovation for the exploitation of ambient energy source.

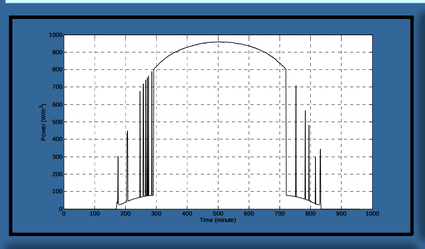
In this poster, we present a new approach to develop power adaptive computing system which can efficiently use energy harvesting from ambient source, and the highlights are:

• a two stage optimization approach for designing power adaptive systems.

• a custom convex model used at run – time to determine clock gating schemes, adjusting system power consumption to instant power supplied from a solar harvester.

2. Research hypothesis and Objective

Figure 1 : The energy harvesting system. It consists of six major components to ensure a robust and stable system performance.

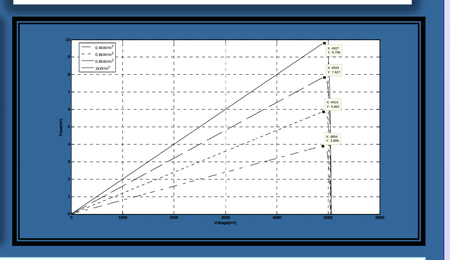


- Energy Harvester

The solar panel results from harvesting the sun radiation on 22/10/2010.

- MPPT

The figure shows that the maximum power points change as solar insolation changes.



For power prediction, we employ a method based on weighted sum of the historical average and previous day's values. The results are shown as follows:

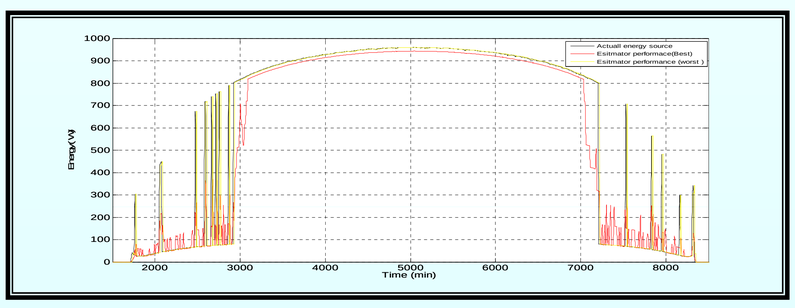


Figure 2: The estimator performance

It can be seen the prediction accuracy is depended on the sample length time, weight value and change rate of weather. Here is the relationship between prediction accuracy (MAPE) and throughput.

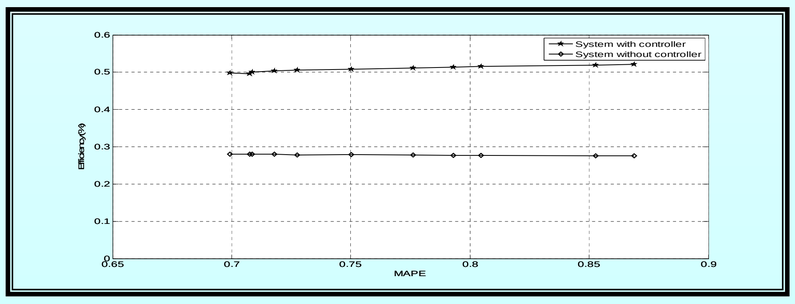
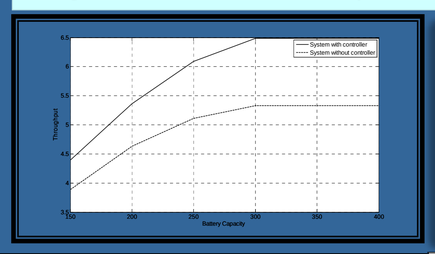


Figure 3: The relationship between MAPE and throughput



- Energy Storage

The design should obey energy neutral operation, which ensures a nominal system operation principle.

For the power adaptive system (Figure 4), a typical dynamic power consumption model for CMOS circuits is

$$P_{ower} = \frac{1}{2} \times V^2 \times C \times f$$

The system works as follows:

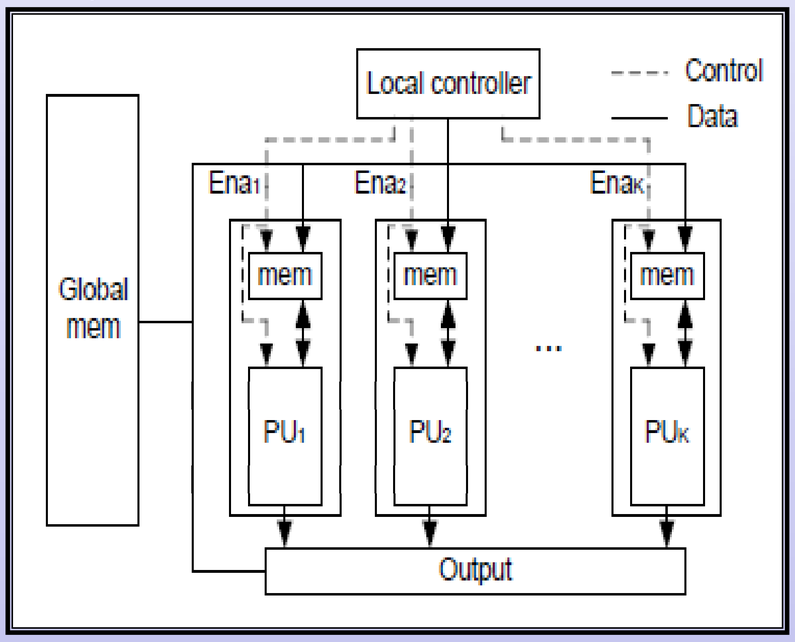


Figure 4: A power adaptive enabled computing system

i. Global memories collected data and stored.

ii. The system controller sends signals to the estimator and run –time optimizer to bring them to work.

iii. The estimator estimates power supply in next 5 minutes and optimizer determine a proper clock gating scheme based on the estimator

iv. The computing system received signals and local controllers triggers data transfers and computing

i. When finish the computing job, the local controller sends back a signal and again.

3. Methodology and Programme

To develop and manage the above described power adaptive system, we propose a two – stage design optimization approach.

Design a parallel computing system for applications with exploitation of data use, loop pipelining and loop parallelization

Design the Run – time optimization: a) a system power model and b) a fast optimizer.

•Design-time optimization

The objective is to minimize the system execution time. The design optimization problem is the following:

$$\min \quad T(\vec{\rho}, \vec{k}, ii)$$

$$\text{subject to} \quad R_{mem}(\vec{\rho}, \vec{k}, ii) \le Res_{ram}$$

$$R_{comp}(\vec{\rho}, \vec{k}, ii) \le Res_{comp}$$

This stage decides the computation structure with the peak speed. However, this peak speed may not be always achievable due to the changing power supplier in the energy harvesting environment.

• Run-time optimization

1) power model: For the parallel computation structure derived in the previous section, the system power consumption variation with different clock gating schemes can be expressed in a model as:

$$P_c = P_{const} + m \times P_{pu}$$

Where the first part is system power loss and PU is a single work unit consumption when experimenting with different clock gating schemes , m is the number of units.

2) Customized optimization model:

A simplified optimization problem is customized from the previous constraints and shown below:

$$\min \quad (v-1) \times t + T_{in}(m) + T_{comp}(m) + T_{out}(m)$$

$$\text{Subject to} \quad \max\left(T_{in}(m), T_{comp}(m), T_{out}(m)\right) \le t$$

$$P_c(m) \le P_s$$

$$1 \le m \le K$$

$$L \times m^{-1} \times v^{-1} \le 1$$

This customized optimization model can be transformed into a convex model, leading to an optimal and fast solution. For the test applications, the system speed is maximum while the system power consumption is not greater than the supplier power.

4. Results and Discussion

In our experiments ,the power adaptive system is evaluated on a hardware platform shown in Fig. 5. The power estimator and system controller are on a ARM926EJ-S processor running at 160*MHz* and having 64MByte SDRAMs, while computation system is mapped onto Virtex5 -330t FPGA with 192 DSP and 324RAM.

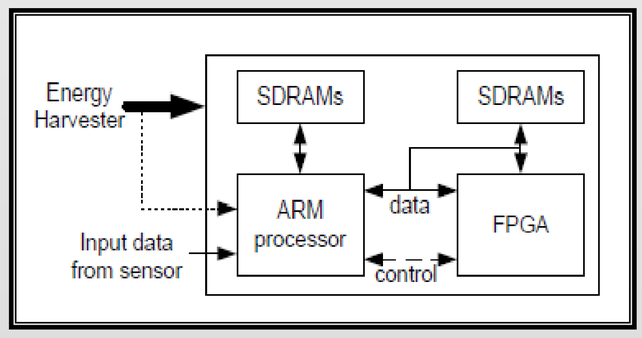


Figure 5: Experimental hardware platform

Three benchmarks are shown:

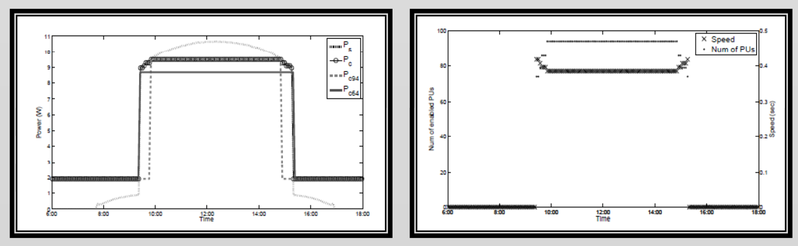


Figure 6: Matrix multiplication

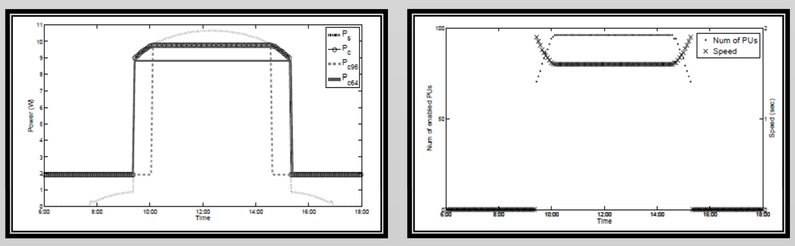


Figure 6: K – means clustering algorithm

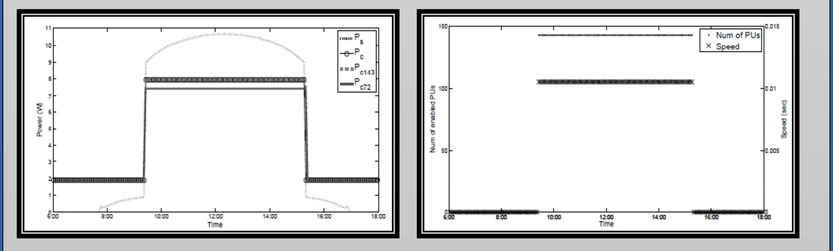


Figure 8: Sobel edge detection

In addition, we also compare two different approaches to determine the clock gating scheme:

Application	Linear power model	Convex model
MAT	14.65 MFLOPS/W	14.73 MFLOPS/W
k-means	11.79 MFLOPS/W	11.79 MFLOPS/W
Sobel	1.27 Mbits/W	1.28 Mbits/W

5. Conclusion and Future work

We present a two-stage optimization approach for designing power adaptive computing systems applied in environments. The purpose is to provide computation capability to nodes in distributed sensor work.

Future work includes improving efficiency and design approach to energy harvesting networks.