Interface Circuit for Piezoelectric Vibration Energy Harvesting System

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1. Introduction

There has been increasing interest in ultra-low power wireless sensors and sensor systems that harvest energy from environmental sources [1]. Small-scale or MEMS-scale vibration energy harvesters and issues surrounding efficient conditioning of the generated electrical power have been the subject of much recent academic research.

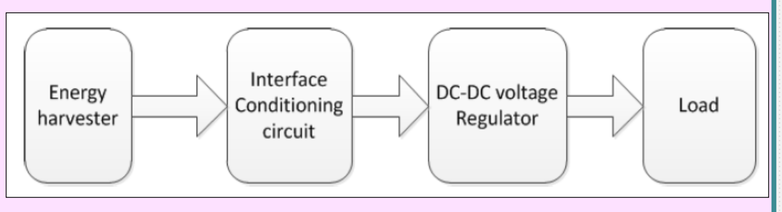

Fig1. System architecture

2. Full-bridge rectifier

The commonly used interface circuit is full-bridge rectifier:

- Less complexity.
- Low power conversion efficiency.
- High threshold

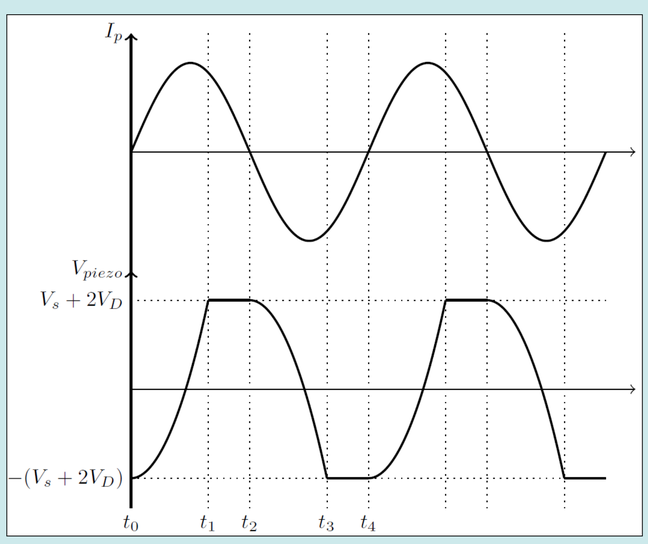

Fig.2: Full-bridge rectifier interface circuit

Figure 1 shows the interface circuit of using a full-bridge rectifier with four diodes. V_D is the forward voltage drop of a diode, V_S is the voltage across the storage capacitor C_S, which is used as an intermediate energy storage capacitor. A battery capacitor C_{BAT} is connected through a bulk DC-DC converter using switches and an inductor.

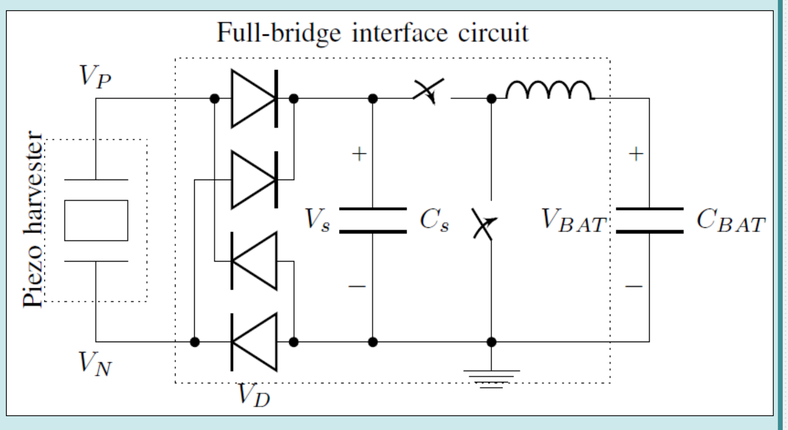

Fig. 3: V_{piezo} waveform

In order to transfer charge from the piezoelectric harvester to the storage capacitor C_S, the voltage across the piezo harvester, note $V_{piezo} = V_P - V_N$, should be higher than a threshold voltage:

$$V_{piezo} > V_S + 2\,V_D$$

or $$V_{piezo} < -(V_S + 2\,V_D)$$

Condition to commence harvesting energy:

$$V_{pp(open)} > 2\,(V_S + 2\,V_D) = V_{TH}$$

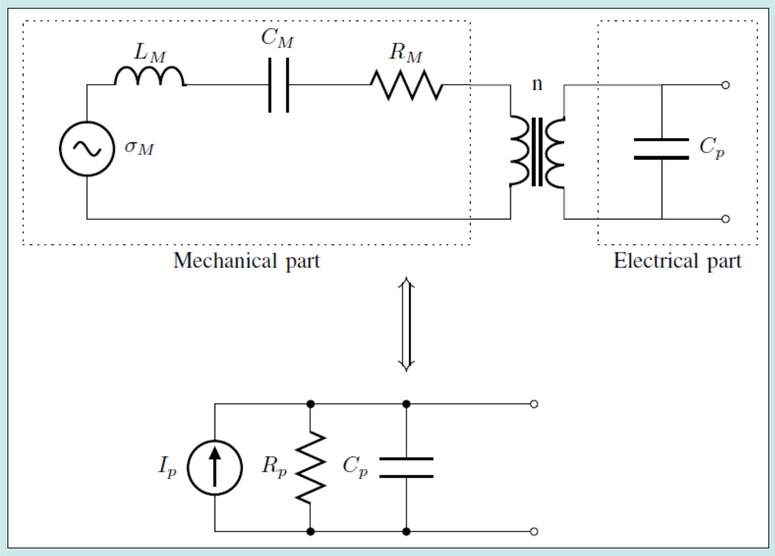

Fig. 4: Equivalent circuit of a piezoelectric harvester

Reasons of this threshold:

- Storage capacitor voltage V_S.
- Diode forward voltage drop V_D.
- Piezo harvester internal capacitor C_p.

Due to this threshold, the amount of charge used to charge C_p is totally wasted and this causes a huge energy loss. Assuming the internal capacitance of piezo harvester is Cp, the charge that wasted in a half vibration cycle is:

$$Q_{wasted} = 2\,C_p\,(V_S + 2\,V_D)$$

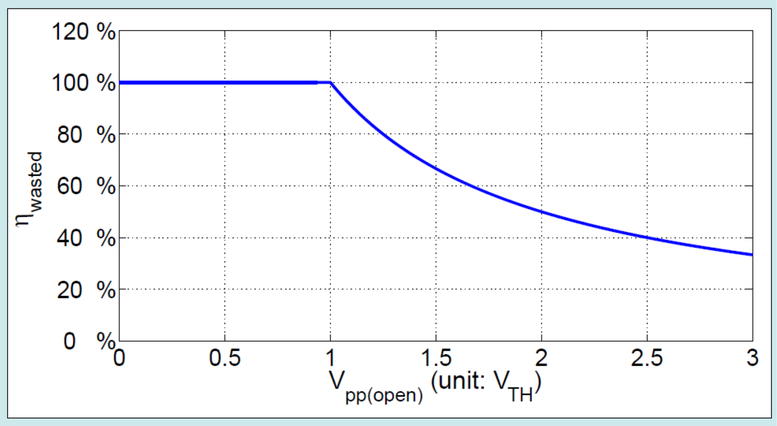

Fig. 5: Percentage of wasted charge

Method of maximizing the power efficiency of the interface circuit:

- Minimize Q_{wasted}
- Minimize power consumption of circuit
- Minimize threshold voltage $2(V_S + 2\,V_D)$

3. Parallel-SSHI interface

P-SSHI (Parallel-Synchronized Switch Harvesting on Inductor) [2] employs an inductor to flip the voltage V_{piezo} to $-V_{piezo}$ in order to minimize the loss due to charging and discharging of C_p.

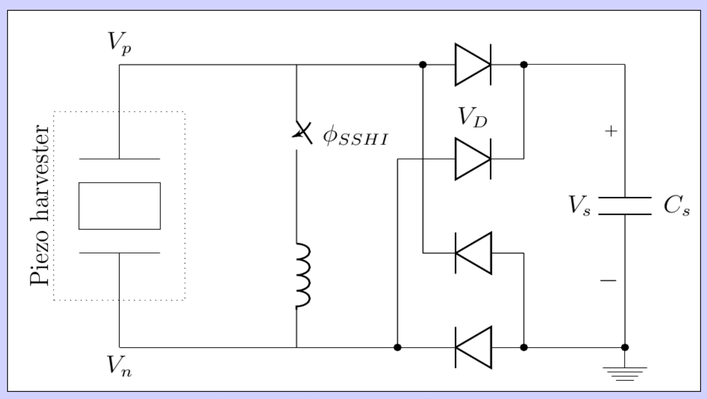

Fig. 6: P-SSHI interface circuit

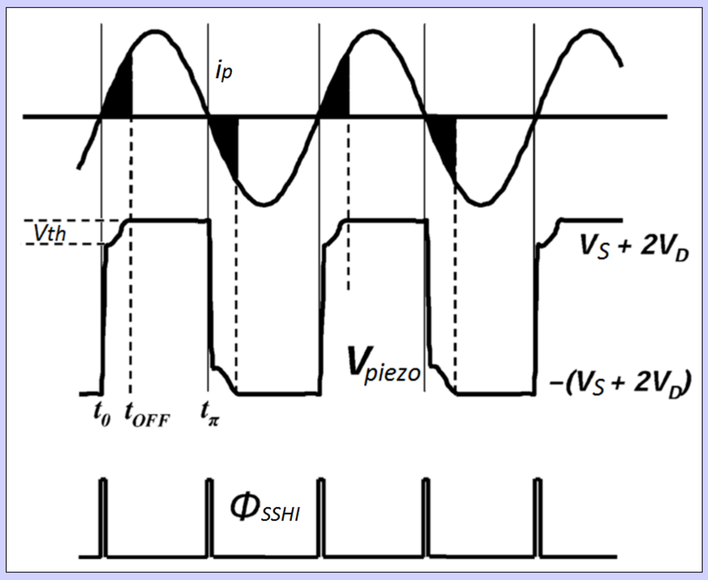

Fig. 7: V_{piezo} waveform using P-SSHI

Advantages of P-SSHI compared to conventional full-bridge rectifier:

- ✓ Charge loss reduced from $2\,C_p\,(V_S + 2\,V_D)$ to $C_p\,V_{th}$
- ✓ Threshold reduced from $2\,(V_S + 2\,V_D)$ to V_{th} (approximately lowered by 80%)

Design consideration:

- Low power consumption.
- High stability.
- Low on-resistance of switch M1 (for higher power conversion efficiency and lower threshold V_{th})

4. Results and conclusion

The P-SSHI interface can significantly improve the power conversion efficiency, especially in small environmental excitations.

Vs	Full-bridge	P-SSHI
1 V	14 µW	23 µW
2 V	7 µW	42 µW
3 V	0	55 µW
4 V	0	63 µW

There are some design challenges:

- Zero current crossing timing (the switch M1 should be turned on exactly when current i_p crosses zero)
- Φ_{BF} pulse width controlling

Other possible ways to increase efficiency:

- Decreasing C_p.
- Using diodes with lower V_D.
- Increasing $V_{pp(open)}$.

References:

[1] S. P. Beeby, M. J. Tudor, and N. M. White, "Energy harvesting vibration sources for microsystems applications," *Measurement Science and Technology,* vol. 17, p. R175, 2006.

[2] Y. K. Ramadass and A. P. Chandrakasan, "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 189-204, 2010.